

Application Information For The UMA1010T/UMA1012T

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Abstract

The UMA1010T and UMA1012T are single chip frequency synthesisers. Both are made with bipolar processing. The UMA1012T is a lower frequency version of the UMA1010, together they offer 50-1100 MHz tuning range. This report describes the application of these devices and gives typical circuit parameters and performance results. Detailed descriptions of the theory behind the circuit elements are given to enable flexible design of synthesisers from first principles.

Application Information For The UMA1010T/UMA1012T

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Summary

This application note covers the design of a phase locked loop based on the Philips UMA1010T or UMA1012T frequency synthesiser. A brief functional description of the devices is given, followed by information covering the full circuit design. The loop filter circuit is covered in detail with all necessary design equations and a worked example is shown.

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1. INTRODUCTION

This report is intended as a guide to designing a phase locked loop based on the Philips UMA1010T or UMA1012T frequency synthesiser integrated circuits. The UMA1010T is a low power single chip solution to frequency synthesis in the range 400MHz to 1100MHz and is primarily intended for use in analog cellular radio applications. The UMA1012T is a lower frequency version of the UMA1012T, operating in the 50MHz-400MHz range. The devices comprise the following functional blocks.

- RF fixed divide by two (UMA1010T only)
- RF dual-modulus prescaler
- RF programmable divider
- Reference oscillator
- Reference programmable divider
- Digital phase comparator
- High gain analog phase comparator
- In-lock detection circuit
- Low noise operational amplifier
- IIC serial programming interface

In addition, the devices feature a power down mode for battery conservation and a XTAL/8 output for use with the Philips cellular radio chipset. The only major external component required is the VCO itself.

This application note presents a design for a frequency synthesiser based on the UMA1010T suitable for the local oscillator for analog cellular radio applications in the 900MHz band. A PCB layout is suggested. The description pertains to the PCAL1122-3 demonstration board available from Philips Components. The design methodology is also directly applicable to the UMA1012T.

For detailed device specifications of the UMA1010T and UMA1012T, refer to the appropriate data sheet.

2. FUNCTIONAL DESCRIPTION OF THE UMA1010T AND UMA1012T

This section provides information on the main functions provided by the UMA1010T and UMA1012T integrated circuits.

2.1. Main Divider Chain

The UMA1012T contains a fully programmable main divider chain with an on-chip RF prescaler. The range of the main divider is from 1024 to 131071 thus permitting all useful phase detector comparison frequencies over the full range of input frequencies.

The UMA1010T has the same divider chain as the UMA1012T, but with an additional fixed divide by two at the RF input to bring the input frequency within the operational range of the fully programmable divider. This means that the actual division ratio is twice the value loaded into the divider register, and that the frequency step size will be twice the phase detector comparison frequency.

Thus for example, to achieve 25kHz channel spacing with a half channel offset with the UMA1010T, the phase detector comparison frequency should be 6.25kHz. A comparison frequency of 12.5kHz would be used with the UMA1012T.

2.2. Reference Divider Chain

Since current analog systems have only a few different channel spacings, and in any system there is a restricted choice of reference crystal frequencies, the UMA1010T and UMA1012T implement a reference divider with limited programmability. A total of 16 different division ratios can be selected which enables all the required phase detector comparison frequencies to be generated. These ratios are 128, 160, 192, 240, 256, 320, 384, 480, 512, 640, 768, 960, 1024, 1280, 1536 and 1920.

In addition, there is one eighth of the crystal frequency available on an output for use with the Philips cellular radio chipset. This chipset uses a 1.2MHz clock for the analog and digital baseband circuits which is provided from the frequency synthesiser; the synthesiser thus requires the use of a 9.6MHz TCXO in this application.

2.3. Phase Detectors

There are three requirements for the phase detector; firstly it should cover the full $\pm 180^\circ$ or $\pm 360^\circ$ phase range, secondly it should have good noise performance, and thirdly it should have good comparison frequency suppression. In order to meet these requirements, the use of two phase detectors is beneficial. The UMA1010T and UMA1012T provide both a digital phase comparator to cover the complete phase range, and a high gain analog phase detector to give good noise performance and comparison frequency rejection.

2.3.1. Digital Phase Comparator

The digital phase comparator is based on D-type flip-flops and thus responds to the full $\pm 360^\circ$ range of phase inputs. During the time when the outputs of the main and reference dividers are out of phase, the comparator either sinks or sources a constant 300 μ A depending on whether the main divider lags or leads the reference divider respectively. Thus, if the VCO frequency is too high, the main divider will increasingly lead the reference divider, the phase comparator will source pulses of current, and the loop filter will correct the VCO error. For a VCO with a characteristic that gives increasing frequency with increasing control voltage, this implies that the loop filter should invert the sense of the phase comparator signal, so a filter based on an inverting op-amp should be used. The gain of the digital phase comparator is hence:

$$PCD \text{ gain} = \frac{300\mu}{2 \times \pi} \text{ A/rad} = 300\mu\text{A/cycle} \quad (1)$$

The digital phase comparator can be programmed to be always on, or to switch off automatically when the analog phase detector described below is in range. The normal use of the synthesiser would program the digital phase comparator to switch off automatically when not required. The digital phase comparator will have a dead-band for very small phase errors due to the finite switch on/ off times of the output charge pump. In practice, this has no effect if the analog phase detector is used in conjunction with the digital phase comparator, since PCD will be disabled for small phase errors. If PCD is being used alone, then the operating point of the loop depends on the circuit used for the loop filter, as various offset voltage and charge leakage effects will move the operating point.

2.3.2. Analog Phase Detector

The high gain analog phase comparator uses the same circuitry as the digital phase comparator to sense the phase relationship of the main and reference dividers, but generates a much higher output signal for the same phase error. This detector thus has a limited operating region, limited by the supply voltage.

At the beginning of the phase comparison cycle, a sampling capacitor is reset to mid-supply. During the time the main and reference dividers are out of phase, the sampling capacitor is charged or discharged from a constant current source depending on whether the main divider leads or lags the reference divider respectively. The current is programmable to one of four values via I²C. At the end of the phase error, the voltage on the sampling capacitor thus depends on the current and the capacitor value. The theoretical final voltage that could be generated on the capacitor without supply voltage limitations also depends on the comparison frequency, as a lower frequency allows more time to charge or discharge the capacitor. The phase detector gain is thus given by:

$$PCA \text{ gain} = \frac{2 \times I_{pccs}}{\pi \times C_{pccs} \times f_c} \text{ V/rad} \quad (2)$$

$$\begin{aligned} \text{where: } I_{pccs} &= \begin{array}{l} 600\mu\text{A} (+6\text{dB}) \\ 378\mu\text{A} (+2\text{dB}) \\ 238\mu\text{A} (-2\text{dB}) \\ 150\mu\text{A} (-6\text{dB}) \end{array} \\ f_c &= \text{comparison frequency} \end{aligned}$$

The voltage on the sampling capacitor is then transferred to a holding capacitor so that the sampling capacitor can be reset to mid-supply ready for the next comparison cycle.

In order to eliminate the effect of the dead-band caused by the detection of phase errors less than the current sink/source switch on/off times, a deliberate small offset is introduced into the phase detector internally. This forces PCA to always have to compensate for this deliberate error, yet has very little effect on the comparison frequency suppression performance.

3. INTERFACING TO THE UMA1010T/UMA1012T

This section details how the UMA1010T or UMA1012T fits into the PLL circuit as shown in Fig.1.

3.1. Programming The UMA1010T/UMA1012T

The UMA1010T and UMA1012T are programmed via the Philips standard I²C bus. To program information into the device registers, it is necessary to transmit first the device address, then a sub-address, and finally the data bytes for the register(s). To read the status register, it is only necessary to transmit the address before reading back the value of the status register. When writing to the UMA1010T or UMA1012T, the sub-address allows writing to any single register, or a burst mode where all registers can be written in one I²C transfer. The formats are thus:

write to one register :

START - address - subaddress - data - STOP

_____ contains register number to be accessed	
_____ R/W bit set to 0 (write)	

write to several registers :

START - address - subaddress - data 1 - ... - data n - STOP

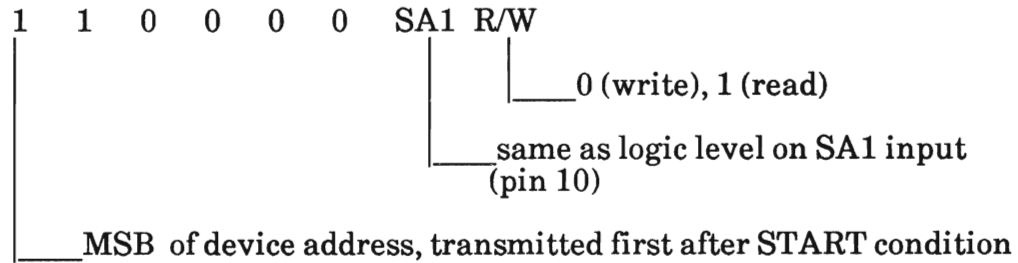
_____ contains first register number to be accessed in the sequence with auto- increment of the register pointer enabled	
_____ R/W bit set to 0 (write)	

read from status register :

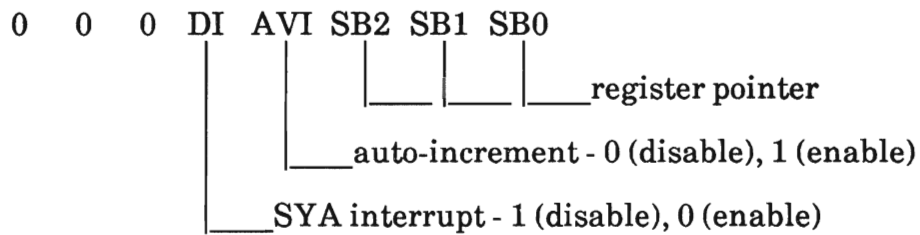
START - address - status - STOP

_____ R/W bit set to 1 (read)

The address byte, in addition to containing the R/W bit as shown above, has one bit that reflects the logic level on the SA1 pin. This allows addressing of up to two synthesiser circuits on the same I²C bus. The format for the address byte is thus:



the subaddress has the following format :



The register map is as follows :

SB 2-0	Bit Allocation								Preset
	7	6	5	4	3	2	1	0	
000	PD	x	x	PCD	RD3	RD2	RD1	RD0	0000 1110
001	VCO1	x	x	VCO0	x	x	x	x	0001 0000
010	x	0	x	x	1	PCG2	PCG1	MD16	1010 1101
011	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	0011 1000
100	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	1000 0000

	0	1
PD	Normal operation	Power down
PCD	PCD auto switch	PCD always on
VCO1	Set VCO1 pin low (pin 12)	Set VCO1 pin high
VCO0	Set VCO0 pin low (pin 11)	Set VCO0 pin high (†1)

RD3...RD0 reference divider programming :

RD3	RD2	Divide by	RD1	RD0	Divide by
0	0	16	0	0	8
0	1	32	0	1	10
1	0	64	1	0	12
1	1	128	1	1	15

The two ratios are multiplied

e.g. RD3...RD0 = 1011 gives divide by $(64 * 15) = 960$

PCG2...PCG1 PCA phase detector gain

PCG2	PCG1	Gain (†2)
0	0	+6dB from nominal
0	1	+2dB from nominal
1	0	-2dB from nominal
1	1	-6dB from nominal

MD16...MD0 main divider value (1024 to 131071, hex \$400 to \$1FFFF)
actual division ratio is $2 * \text{divider value}$ for UMA1010T

- (†1) The VCO0 pin is forced low during an out-of-lock condition
- (†2) The nominal gain is determined by the comparison frequency and the value of the capacitor connected to the PCCS pin (pin 23).

The status register contains the following information :

Bit Allocation							
7	6	5	4	3	2	1	0
0	0	0	OOL	0	LOOL	LPD	DI

	0	1
OOL	Normal state	Momentarily out-of-lock
LOOL	Normal state	Latched out-of-lock (†)
LPD	Normal state	Latched power dip (†)
DI	Interrupt enables on SYA	Interrupt disabled on SYA

(†) These are cleared after reading the status register, assuming that the error condition has been removed.

It should be noted that any I²C transfers to the synthesiser will cause momentary interference to be generated on the phase detector output, hence giving spurious signals on the VCO output if the synthesiser is in an operational locked state. These spurious signals reflect the current pulses within the device to pull the SDA line low during acknowledge clock cycles or transmission of the status register. Any I²C bus activity not addressing the synthesiser should not cause any interference from this effect, so in normal operation this interference is not a problem.

3.2. Hardware Control Inputs And Outputs

There are a number of status and control signals generated by the UMA1010T and UMA1012T, and also a hardware control input. This section describes the function of each of these.

3.2.1. HPD Input

This input is used to disable the divider chains in order to save power when the synthesiser is not required to be operational. The power down state can be activated by either taking this pin low or by setting the power down bit in the I²C register to a '1'. The input has an internal pull-up resistor so that normal operation will be obtained if the pin is left open circuit.

The power down state does not have any effect on the I²C circuitry, so that the device may still be addressed, and new information programmed into the registers even in the power down mode.

3.2.2. FX8 Output

This is an open collector output of one eighth of the crystal or TCXO input frequency. It is required for use with the Philips cellular radio chipset for AMPS and TACS systems; in this application the synthesiser should be used with a 9.6MHz TCXO. The recommended pull-up load is 27kΩ.

3.2.3. SYA (Synthesiser Alarm) Output

This is an open collector output which is normally held high by an external 27k Ω load. Under error conditions, the synthesiser forces SYA low. The error conditions that set SYA low are a power dip or an out-of-lock condition (PCA out of range). SYA is reset again by reading the status register, which contains the relevant alarm information. The SYA output can also be enabled and disabled via I²C as required.

The typical use of SYA would be to interrupt a microcontroller to warn of the error condition. As the output is open collector, it is possible to connect more than one device together directly; in this case the microcontroller would poll the relevant devices to locate the source of the error condition.

3.2.4. VCO0 And VCO1 Outputs

These are open collector outputs and are intended for enabling the power supply to VCOs or buffer stages so that these parts of the set can be powered down when not required to be operational. The outputs are controlled via I²C. In addition, the VCO0 output is forced low during an out-of-lock condition; this output could therefore be used to disable the transmitter of the set when this condition occurs to prevent causing interference to other sets. In this case, there may well be other parts of the circuitry also controlling the transmitter in the same way; as the VCO0 and VCO1 lines are open collector, they may be directly connected to other such controlling signals.

The VCO1 output is not affected by the hardware power down input or power down via I²C. The VCO0 output will of course be forced low due to the out-of-lock condition resulting from a power down.

3.3. Crystal Oscillator

For analog cellular radio applications, the UMA1010T will almost certainly be used with an external oscillator in order to provide the stability necessary to ensure operation within the specification. However, in case some other applications do not require such accuracy, provision has been made to form a crystal oscillator using the RI1 and RI2 inputs (pins 3 and 2 respectively). The oscillator circuit should be of the Colpitts type and thus requires the addition of three capacitors to function. This is shown in Fig.2. with capacitor values suitable for operation at 9.6MHz.

The internal biasing provides possible operation over the range 3MHz to 16MHz with the addition of a suitable crystal. It may be necessary to adjust the values of the capacitors slightly to guarantee oscillation under all conditions for frequencies significantly different to 9.6MHz.

The crystal used in this circuit is series resonant, fundamental mode, with a load capacitance of approximately the series combination of the three capacitors.

3.4. External Oscillator

When using an external oscillator such as a TCXO module, the output from the oscillator should be connected directly to the RI1 pin (pin 3). The RI2 pin (pin 2) should either be left open circuit, or could be used as a buffered version of the signal applied to RI1.

3.5. PCA Gain Setting

The equation below giving the gain of PCA is repeated from section 2.3.2. and converted from a gain in V/rad to V/cycle

$$K\phi = \frac{4 \times Ipccs}{Cpccs \times fc} = V/cycle \quad (3)$$

$$\begin{aligned} \text{where: } Ipccs &= 600\mu A \quad (+6dB) \\ &378\mu A \quad (+2dB) \\ &238\mu A \quad (-2dB) \\ &150\mu A \quad (-6dB) \\ fc &= \text{comparison frequency} \end{aligned}$$

Cpccs has a recommended range of 60pF to 200pF. Values outside this range will not give the expected gain since for very low values of Cpccs, the stray capacitance starts to have an effect; for higher values of Cpccs, the circuit that resets the capacitor to mid-supply may not work effectively due to its limited current handling capability.

As an example, with a comparison frequency of 6.25kHz, gain programmed to +2dB and Cpccs equal to 100pF, PCA gain will be 385V/rad or 2419V/cycle.

In general, it is best to choose a high gain for PCA to give the best noise performance since the noise output from PCA is independent of the gain, and a higher PCA gain requires a lower gain in the loop filter. The lower loop filter gain results in less phase detector noise being mapped onto the VCO output. However, when PCA and PCD are combined into one loop filter, the high gain of PCA may require an unreasonably large input resistor from PCA into the loop filter. This can be reduced either by reducing PCA gain and accepting a worse close-in noise performance, or by adjusting the loop filter components to give lower resistor values and higher capacitor values to keep the time constants for PCA correct. This does, however, alter the gain time constant for PCD since this is determined differently; this results in a lower bandwidth for PCD which increases the lock time.

3.6. Loop Filter Design

The correct design of the loop filter is of considerable importance for the optimum performance of the synthesiser. The filter should be designed so as to achieve the required compromise between noise performance and switching time, and so the actual circuit used will depend on the particular application

The recommended loop filter schematic is given in Fig.3; this is a third order filter for the PCA loop, and fourth order for the PCD loop. Although this is more complex to design than the common second order loop, it does have advantages:

- The additional capacitor in the op-amp feedback path aids stability of the op-amp itself.
- The RC stage on the VCO control line is useful to filter out any op-amp noise.
- The RC on PCD before the op-amp reduces the bandwidth of this signal giving better transient performance.
- The higher resultant filter order gives improved suppression of comparison frequency breakthrough components.

The disadvantages are of course slightly increased circuit complexity and additional design work. The best design method is based on the classic equations for the second order filter which generates the three required time constants from the desired values for loop bandwidth (f_n Hz) and phase margin (ϕ_m degrees) shown below:

$$\omega_n = 2 \times \pi \times f_n \text{ rad/s} \quad (4)$$

$$\tau_3 = \frac{1}{\omega_n} \times \left\{ \frac{1}{\cos(\phi_m)} - \tan(\phi_m) \right\} \quad (5)$$

$$\tau_2 = \frac{1}{\omega_n^2 \times \tau_3} \quad (6)$$

$$\tau_1 = \frac{K_v \times K_f}{N \times \omega_n^2} \times \sqrt{\frac{\tau_2}{\tau_3}} \quad (7)$$

Note that the units of K_v and K_c should be correct :

either K_c in V/rad, K_v in rad/sec/Volt) for
or K_c in V/cycle, K_v in Hz/Volt) PCA

either K_c in A/rad, K_v in rad/sec/Volt) for
or K_c in A/cycle, K_v in Hz/Volt) PCD

The loop bandwidth is usually chosen from switching time considerations, and can be approximated to:

$$f_n = \frac{3}{\text{switching time}} \text{ Hz} \quad (8)$$

The phase margin would normally be chosen to be around 45° to 50°, but we must make allowances for the presence of additional time constants in the circuit compared to the second order filter. In addition, when designing for the PCA loop, we must take into account the action of the sample and hold integral to PCA. These allowances mean that we should use a higher phase margin in the equation for τ_3 above, and also give a gain reduction in the equation for τ_1 above. It is recommended that the PCA loop is designed for about 50° phase margin and the PCD loop about 45° phase margin, before taking the effects just described into account.

The phase shift and gain change due to each addition time constant in the filter are:

$$\phi_{\tau} = \tan^{-1} (\omega \times \tau) \text{ degrees} \quad (9)$$

$$K_{\tau} = \frac{1}{\sqrt{1 + (\omega \tau)^2}} \quad (10)$$

The phase shift and gain change due to the sample and hold are:

$$\phi_{sh} = \frac{180 \times f_n}{f_c} \text{ degrees} \quad (11)$$

$$K_{sh} = \frac{\sin(\phi_{sh})}{\pi \times f_n / f_c} \quad (12)$$

Thus in calculating the time constants, we should use the sum of the phase shifts and the desired resultant phase margin in the equation for τ_1 above. We must also apply the gain correction as shown below:

$$\phi_{m'} = \phi_m + \phi_{sh} + \sum \phi_{\tau} \text{ degrees} \quad (13)$$

i.e. $\phi_{m'}$ is the sum of all the phase shifts.

$$K_c = K_{sh} \times \prod K_{\tau} \quad (K_c < 1) \quad (14)$$

i.e. K_c is the product of all the gain reductions.

This value for $\phi_{m'}$ is then used in the equation above for τ_3 , and the gain correction K_c is applied to the equation for τ_1 as shown below so that τ_1 is reduced due to the effects of the additional filter order(s) and the sample-and-hold

$$\tau_3 = \frac{1}{\omega n} \times \left\{ \frac{1}{\cos(\phi m')} \right\} - \tan(\phi m') \quad (15)$$

$$\tau_2 = \frac{1}{\omega n^2 \times \tau_3} \quad (16)$$

$$\tau_1 = \frac{Kc \times Kv \times K\phi}{N \times \omega n^2} \times \sqrt{\frac{\tau_2}{\tau_3}} \quad (17)$$

In designing the higher order filter, the additional time constants should be chosen to be rather higher than the loop bandwidth, and the phase margin $\phi m'$ above must of course be limited to be somewhat less than 90° . It is recommended that the following conditions are adhered to:

$$\phi m' \leq 80^\circ \quad (18)$$

$$each \ \phi \tau \leq 22^\circ \text{ at } \omega n \quad (19)$$

So for a 4th order filter with sample and hold we would have:

$$\phi m + \phi \tau_4 + \phi \tau_5 + \phi sh \leq 80^\circ \quad (20)$$

Having used the above equations to determine all the necessary time constants, the circuit itself must be determined. Refer to Fig.3 for the circuit configuration for a 3rd/4th order filter - this is the most complex filter that we shall consider here. There are five time constants which will relate to τ_1 to τ_3 for the second order design and τ_4 to τ_5 for the additional two filter orders. The equations for these are:

$$\tau_a = R1 \times (C2 + C3) \quad PCA - \text{voltage output} \quad (21)$$

$$\tau_a = (C2 + C3) \quad PCD - \text{current output} \quad (22)$$

$$\tau_b = R3 \times (C2 + C3) \quad (23)$$

$$\tau_b = R4 \times C4 \quad (24)$$

$$\tau_d = R3 \times C3 \quad (25)$$

$$\tau_e = R2 + C1 \quad PCD - \text{current output} \quad (26)$$

We now need to re-arrange the equations slightly to give the component values from the time constants rather than vice versa for circuit design purposes. This gives the following:

$$C2 \text{ arbitrarily chosen} \quad PCA - \text{voltage output} \quad (27)$$

$$C2 = \tau_a \times (\tau_b - \tau_d) / \tau_b \quad PCA - \text{voltage output} \quad (28)$$

$$R3 = (\tau_b - \tau_d) / C2 \quad (29)$$

$$C4 \text{ arbitrarily chosen} \quad (30)$$

$$R4 = \tau_c / C4 \quad (31)$$

$$C3 = \tau_d / R3 \quad (32)$$

$$C1 \text{ arbitrarily chosen} \quad (33)$$

$$R1 = \tau_a / (C2 + C3) \quad PCA - \text{voltage output} \quad (34)$$

$$R2 = \tau_e / C1 \quad PCA - \text{voltage output} \quad (35)$$

Thus, we first choose arbitrary (but sensible) values for C4 and C1 and determine the remaining filter components from the design equations.

For simpler circuit configurations, we can use the same equations with the following conditions:

$$C3 = 0 \text{ and/or } R4 = C4 = 0 \quad (36)$$

The relationship between τ_1 to τ_5 and τ_a to τ_e is then:

$$\tau_1 = \tau_a \quad (37)$$

$$\tau_2 = \tau_b \quad (38)$$

$$\tau_3 = (\tau_c \mid \tau_d \mid \tau_e) \quad (39)$$

$$\tau_4 = (\tau_c \mid \tau_d \mid \tau_e) \neq \tau_3 \quad (40)$$

$$\tau_5 = (\tau_c \mid \tau_d \mid \tau_e) \neq \tau_4 \neq \tau_3 \quad (41)$$

i.e. we can choose any one-to-one mapping for $\tau_3.. \tau_5$ to $\tau_c.. \tau_e$.

In general it is best to choose τ_3 for the time constant on the op-amp output ($R_4 \times C_4$) if these components are present, since this provides maximum filtering of any op-amp output noise.

3.6.1 Worked Example

As an example, we will design the loop filter for the UMA1010T under the conditions shown below. This design is not the same as the circuit given on the PCAL1122-1 demonstration board, but is more suitable for an AMPS cellular radio application.

VCO frequency	=	825 MHz - 845 MHz
VCO gain	K_v	= 11 MHz/V
Channel spacing	=	30 kHz, with no half channel offset
Reference oscillator	=	9.6 MHz
Switching time	<	20 msec

Since there is no half channel offset, we should choose a comparison frequency of 15kHz to give the required 30kHz step with the UMA1010T. We shall now choose a loop bandwidth f_n of around 200Hz to satisfy the switching time requirements, giving $\omega_n = 1257$ rad/sec. We will use the loop filter configuration shown in Fig.3 and design for 50° phase margin for the PCA loop and provide approximately 45° phase margin for the PCD loop.

First we will relate the five time constants to the circuit as in the figure. From the equations above giving the time constants of the circuit we shall choose the following mapping:

We shall now consider the design for PCA. We will choose to have PCA gain programmed to +2dB, giving $I_{pccs} = 378\mu A$, and $C_{pccs} = 100pF$. With a comparison frequency of 15kHz, this gives PCA gain as 1007V/cycle. The analog phase detector comprises a sample-and-hold, so we obtain the following corrections for this:

$$\phi_{sh} = 2.4^\circ \quad (48)$$

$$K_{sh} = 0.9997 \quad (49)$$

We shall choose to allow about 20° phase shift in the additional RC of the loop filter for PCA, giving:

$$\phi_{v4} = 20^\circ \quad (50)$$

$$\text{thus } \tau_4 = 289.6\mu sec \quad (51)$$

$$K_{\tau 4} = 0.9396 \quad (52)$$

So we must design for a phase margin of:

$$\phi m' = 50^\circ + 2.4^\circ + 20^\circ = 72.4^\circ \quad (53)$$

Before continuing the calculation, we should consider the design for PCD since PCD has an extra filter order, no sample-and-hold, and is a current output with a different equation for τ_1 . Note that τ_2, τ_3, τ_4 will be the same for the PCA loop as for the PCD loop, but τ_1 will differ, and of course the PCD loop will have a τ_5 . τ_5 will thus have to be allocated to the RC section on the output of PCD. Now, since τ_2 and τ_3 determine the phase margin of the loop, we cannot alter the designed phase margin $\phi m'$ chosen for the PCA loop. We will allow a further 10° phase shift in the additional RC section, so that:

$$\phi \tau_5 = 10^\circ \quad (54)$$

$$\text{thus } \tau_5 = 140.3 \mu\text{dsec} \quad (55)$$

$$K \tau_5 = 0.9848 \quad (56)$$

The actual phase margin that the PCD loop will have is then given from:

$$\phi m' = 72.4^\circ = \phi m + 20^\circ + 10^\circ \quad (57)$$

$$\text{thus } \phi m = 42.4^\circ \quad (58)$$

so the PCD loop will have 42.4° phase margin at the design loop bandwidth, which is an acceptable value. Using the equations given above, we then calculate:

$$\tau_5 = 140.3 \mu\text{s} \quad (59)$$

$$\tau_4 = 289.6 \mu\text{s} \quad (60)$$

$$\begin{aligned} \tau_3 &= \frac{1}{1257} \times \left\{ \frac{1}{\cos(72.4)} \right\} - \tan(72.4) \\ &= 123.2 \mu\text{s} \end{aligned} \quad (61)$$

$$\tau_2 = \frac{1}{1257^2 \times 123.2\mu} \quad (62)$$

$$= 5.139\text{ms}$$

$$\tau_1 = \frac{0.9396 \times 11M \times 1007}{(835M/15k) \times 1257^2} \times \sqrt{\frac{5.139m}{123.2\mu}} \quad (63)$$

$$= 764.4\text{ms} \quad (\text{PCA})$$

$$\tau_1 = \frac{0.9396 \times 0.9848 \times 11M \times 300\mu}{(835M/15k) \times 1257^2} \times \sqrt{\frac{5.139m}{123.2\mu}} \quad (64)$$

$$= 224.3\text{ns A/V} \quad (\text{PCD})$$

From the equations given above, we are forced to use a certain value for (C2 + C3) so that τ_1 is correct for PCD. Thus we have:

$$C2 = 224.3n \times (5.139m - 289.6\mu) / 5.139m = 211.7\text{nF} \quad (65)$$

$$R3 = (5.139m - 289.6\mu) / 211.7n = 22.9\text{k}\Omega \quad (66)$$

$$C4 \text{ (chosen arbitrarily)} = 10\text{nF} \quad (67)$$

$$R4 = 123.2\mu / 10n = 12.3\text{k}\Omega \quad (68)$$

$$C3 = 289.6\mu / 22.9k = 12.6\text{nF} \quad (69)$$

$$C1 \text{ (chosen arbitrarily)} = 10\text{nF} \quad (70)$$

$$R1 = 764.4m / 211.7n + 12.6n = 3.41\text{M}\Omega \quad (71)$$

$$R2 = 140.3\mu / 10n = 14\text{k}\Omega \quad (72)$$

To complete the design, these values should be rounded to the nearest values from the E12 or E24 series as appropriate. If desired, the effects of this rounding can be calculated, and if the actual loop bandwidth and phase margins differ too much from the intended values, suitable adjustments can be made to give a more accurate result. However, in most cases this will not be needed.

3.7 PCB Layout Considerations

The circuit of the UMA1010T demonstration board (PCAL1122-3) is shown in Fig.4, with the layout shown in Fig.5. This PCB has a solid ground plane on one side (apart from isolated pads for non-grounded connections to leaded components). In addition, there are areas of ground plane on the surface mount side of the board to ensure satisfactory grounding of important components. There are a good number of plated-through holes connecting the two layers of ground plane. Normal RF design practices should of course be taken into account when laying out the circuit. There are a number of particular points that should be borne in mind when considering the circuit and layout

- The non-surface mount side of the board (if a two-sided board is used) should be virtually solid ground plane to give good RF performance.
- The 5V digital supply (Vp) should be well decoupled as close to the pin as possible, preferably with a large value capacitor (e.g. 47 μ F) in parallel with a smaller value ceramic (e.g. 100nF).
- The 5V analog supply (Vp1) should be well isolated from the 5V digital supply. This can be achieved with an RC circuit in the 5V analog supply since only a small current is required. Routing the 5V supply between Vp and Vp1 under the IC is to be avoided.
- Incorporating a ground plane on the surface mount side of the PCB underneath the synthesiser helps isolate digital noise from the analog parts. This ground plane should be well connected with vias to the full ground plane.

4. TYPICAL PERFORMANCE

This section describes the typical performance obtainable with the UMA1010T with regard to the PCAL1122-3 demonstration board. The relevant performance criteria for a synthesiser are usually:

- Close-in phase noise (i.e. noise within the loop bandwidth)
- Noise floor at an offset from the carrier
- Comparison breakthrough components
- Switching time

It should be noted of course that these criteria can be traded off against each other to some extent to tailor the overall performance, and that the performance described here is only one compromise between the various criteria. In general, the choice of a low loop bandwidth will improve the comparison frequency breakthrough and will filter out more of the close-in phase noise, but will result in a longer switching time. The use of a higher order filter can improve comparison frequency breakthrough with little effect on the noise or switching time. The noise floor at offsets significantly higher than the loop bandwidth are determined completely by the VCO itself with a loop filter configuration that has low pass filtering on the filter op-amp output.

Plots of the close-in spectrum (span of 2kHz) and also a span of 50kHz are shown in Figs 6 and 7 respectively for a carrier frequency of 1GHz and a comparison frequency of 6.25kHz. From Fig.6 we can see that the loop bandwidth is around 300Hz, and Fig.7 shows the VCO noise floor at offsets greater than about 15kHz from the carrier with the first and second comparison frequency breakthrough component being visible at 6.25kHz and 12.5kHz from the carrier respectively.

Figure 8 shows switching waveforms for a frequency jump of 5MHz. The top trace (labelled Ch1) is the I²C transfer to the UMA1010T; the second (Ch2) is the VCO1 output showing the out-of-lock condition. The third trace (Ch3) is the VCO control line. The fourth trace (Ch4) is the RF output of the VCO mixed down to 0Hz with a signal generator at the destination frequency. The VCO output is isolated from the mixer with an amplifier with 30dB gain followed by a 30dB attenuator. The mixer output trace shows that the switching time is around 16msec, which is a little longer than the VCO control line trace appears to show. This is because observation of the VCO control line is not accurate due to the very high VCO gain - with say 10MHz/V sensitivity, to measure to within 1kHz of destination frequency requires resolving the VCO control line to within 100µV which is clearly very difficult.

From this figure, we can see that the VCO control line has a single overshoot during switching; this shows that the loop is properly damped, so the phase margin is correct.

To summarise the performance of the circuit in the figures:

Loop bandwidth	300Hz
Close-in noise	-45dBc/Hz at 200Hz from carrier
VCO noise floor	-118dBc/Hz at 25kHz from carrier
Residual FM	33Hz RMS, CCITT weighted
Comparison frequency breakthrough	-63dBc at 6.25kHz -79dBc at 12.5kHz
Switching time	16msec for 5MHz jump

5. CONCLUSIONS

Information regarding the use of the UMA1010T/UMA1012T in a frequency synthesiser application has been presented. A detailed methodology for determining the loop filter components has been described since the switching and noise performance of the complete circuit depends on a good filter design. The layout of the PCAL1122-3 demonstration board has been shown as an example PCB layout.

6. REFERENCES

1. UMA1010T Preliminary Data Sheet, September 1988 (†)
2. Ulriche, L. Rohde; Digital PLL Frequency Synthesisers Theory and Design.
3. N.M.W. Oatley; Application Information For The TDD1742T, MCO/AN89002.

(†) At the time of writing, a new issue of the UMA1010T data sheet and the first issue of the UMA1012T data sheet were being prepared.

APPENDIX A

LOOP FILTER DESIGN EQUATIONS

The necessary equations for the design of the loop filter are repeated here for quick reference. Refer to Fig.3 for the circuit configuration.

- Determine the loop bandwidth from:

$$f_n = \frac{3}{\text{switching time}} \text{ Hz} \quad (8)$$

- Choose the phase margin ϕ_m for PCA (50° recommended)
- Determine the phase shift and gain correction for the sample-and-hold for PCA

$$\phi_{sh} = \frac{180 \times f_n}{f_c} \text{ degrees} \quad (11)$$

$$K_{sh} = \frac{\sin(\phi_{sh})}{\pi \times f_n / f_c} \quad (12)$$

- Choose the phase shift $\phi_{\tau 4}$ to be allowed in the additional time constant for PCA and PCD, and the resultant design phase margin ϕ_m' from:

$$\phi_{\tau 4} \leq 22^\circ \text{ at } \omega_n \quad (19)$$

$$\phi_m' = \phi_m + \phi_{sh} + \phi_{\tau 4} \text{ degrees} \quad (13)$$

$$\phi_m' \leq 80^\circ \quad (18)$$

- determine $\tau 4$ using

$$\phi_{\tau 4} = \tan^{-1}(\omega_n \times \tau 4) \text{ degrees} \quad (9)$$

- determine the gain correction for $\tau 4$ from:

$$K_{\tau 4} = \frac{1}{\sqrt{1 + (\omega_n \times \tau 4)^2}} \quad (10)$$

- Calculate the gain correction K_c for PCA from:

$$K_c(PCA) = K_{sh} \times K_{\tau 4} \quad (K_c < 1) \quad (14)$$

- Choose the phase shift $\phi_{\tau 5}$ to be allowed in the additional time constant for PCD giving the resultant phase margin ϕ_m for the PCD loop:

$$\phi_{\tau 4} \leq 20^\circ \text{ at } \omega_n \quad (19)$$

$$\phi_m'(PCD) = \phi_m' - (\phi_{\tau 4} + \phi_{\tau 5}) \text{ degrees} \quad (\text{from 13})$$

- Determine τ_5 using:

$$\phi_{\tau 5} = \tan^{-1}(\omega_n \times \tau_5) \text{ degrees} \quad (9)$$

- Determine the gain correction for τ_5 from:

$$K_{\tau 5} = \frac{1}{\sqrt{1 + (\omega_n \times \tau_5)^2}} \quad (10)$$

- Calculate the gain correction K_c for PCD from:

$$K_c(PCD) = K_{\tau 4} \times K_{\tau 5} \quad (K_c < 1) \quad (14)$$

- Calculate ω_n from f_n :

$$\omega_n = 2 \times \pi \times f_n \text{ rad/s} \quad (4)$$

- Choose the gain for PCA according to the setting programmed via I²C and the C_{pccs} capacitor

$$K_\phi = \frac{4 \times I_{pccs}}{C_{pccs} \times f_c} = V/\text{cycle} \quad (3)$$

$$\begin{aligned} \text{where: } I_{pccs} &= \begin{array}{l} 600\mu A \quad (+6dB) \\ 378\mu A \quad (+2dB) \\ 238\mu A \quad (-2dB) \\ 150\mu A \quad (-6dB) \end{array} \\ f_c &= \text{comparison frequency} \end{aligned}$$

- Calculate the standard second order filter time constants from:

$$\tau_3 = \frac{1}{\omega n} \times \left\{ \frac{1}{\cos(\phi m')} - \tan(\phi m') \right\} \quad (15)$$

$$\tau_2 = \frac{1}{\omega n^2 \times \tau_3} \quad (16)$$

$$\tau_1 = \frac{K_c(PCA) \times K_v \times K_\phi}{N \times \omega n^2} \times \sqrt{\frac{\tau_2}{\tau_3}} \quad (\text{for PCA}) \quad (17)$$

$$\tau_1 = \frac{K_c(PCD) \times K_v \times K_\phi}{N \times \omega n^2} \times \sqrt{\frac{\tau_2}{\tau_3}} \quad (\text{for PCD}) \quad (17)$$

- Determine the filter components from:

$$C_2 = \tau_1(PCD) \times (\tau_2 - \tau_4) / \tau_2 \quad (28)$$

$$R_3 = (\tau_2 - \tau_4) / C_2 \quad (29)$$

$$C_4 \text{ arbitrarily chosen} \quad (30)$$

$$R_4 = \tau_3 / C_4 \quad (31)$$

$$C_3 = \tau_4 / R_3 \quad (32)$$

$$C_1 \text{ arbitrarily chosen} \quad (30)$$

$$R_1 = \tau_1(PCA) / (C_2 + C_3) \quad (34)$$

$$R_2 = \tau_5 / C_1 \quad (35)$$

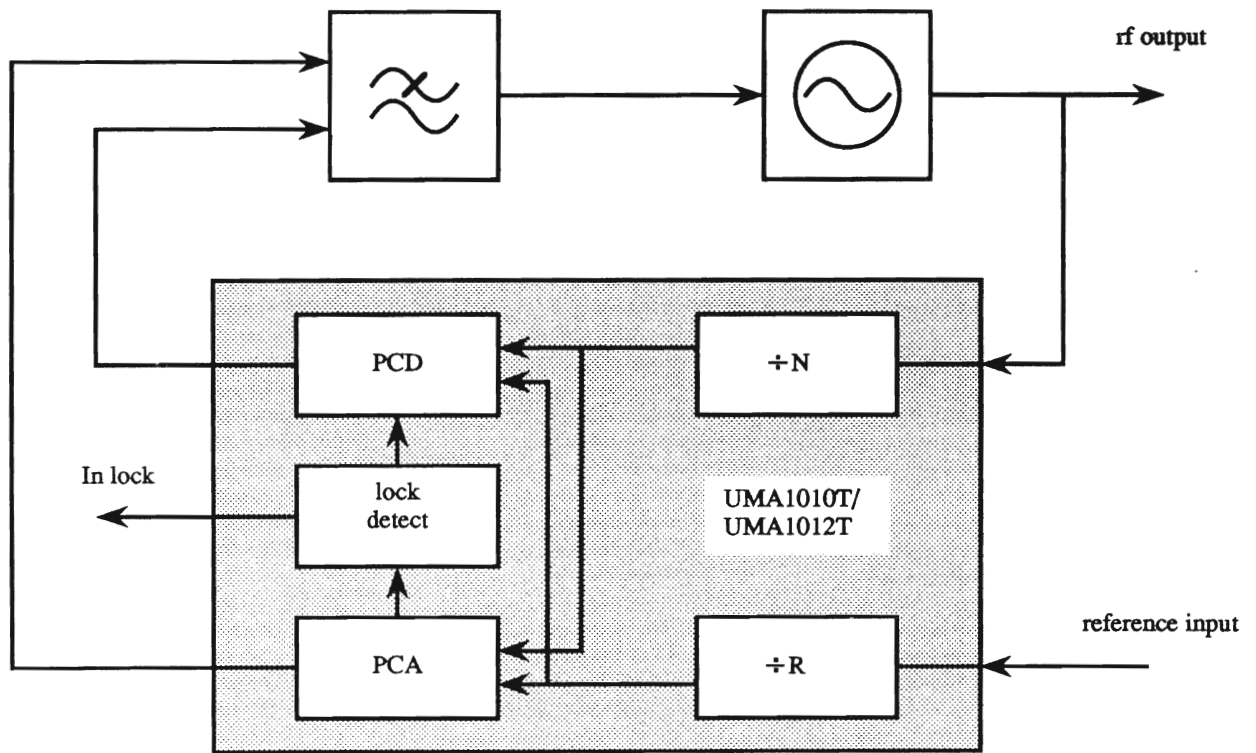


Figure 1 PLL circuit block diagram

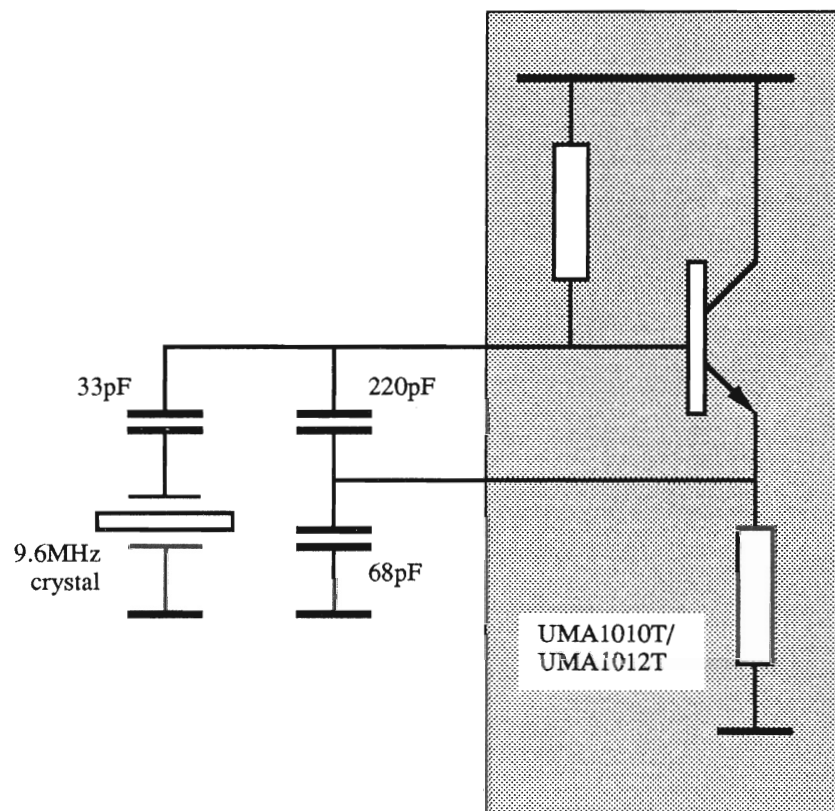


Figure 2 Crystal oscillator circuit

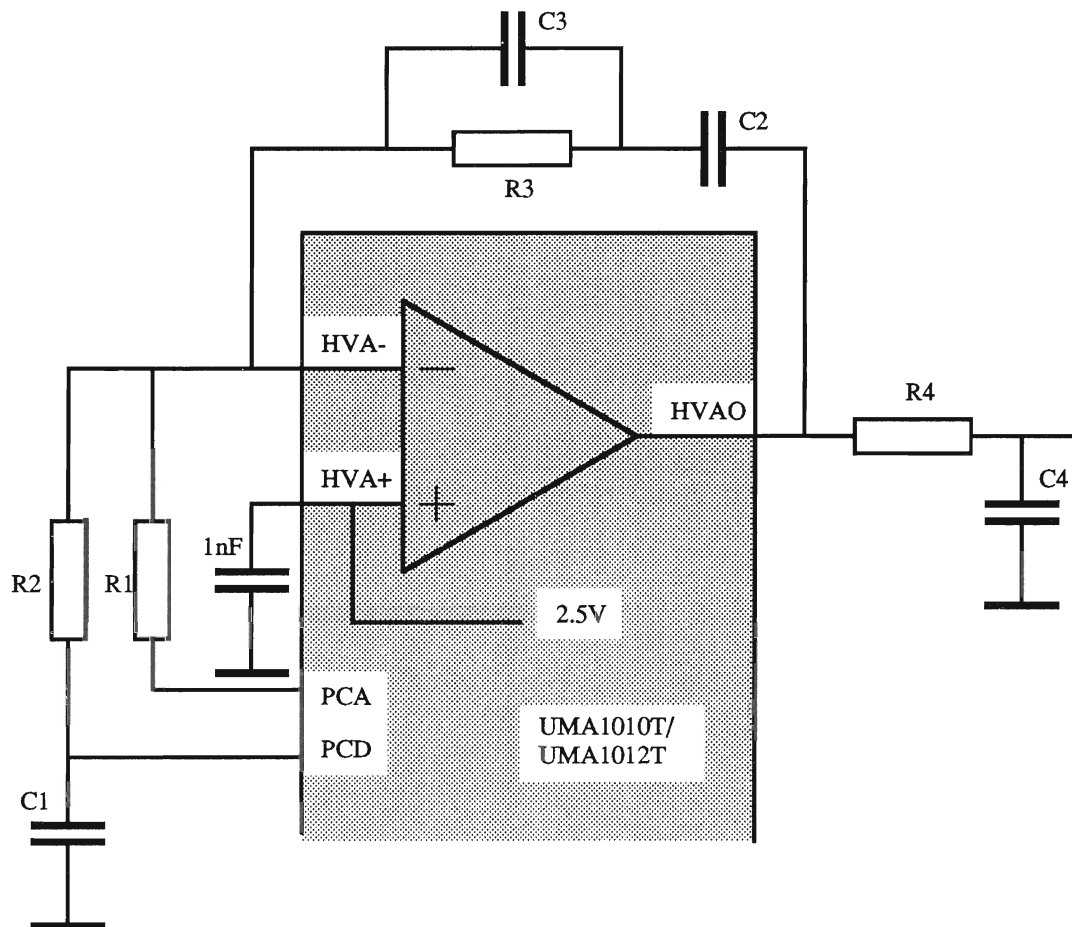


Figure 3 Loop filter circuit diagram

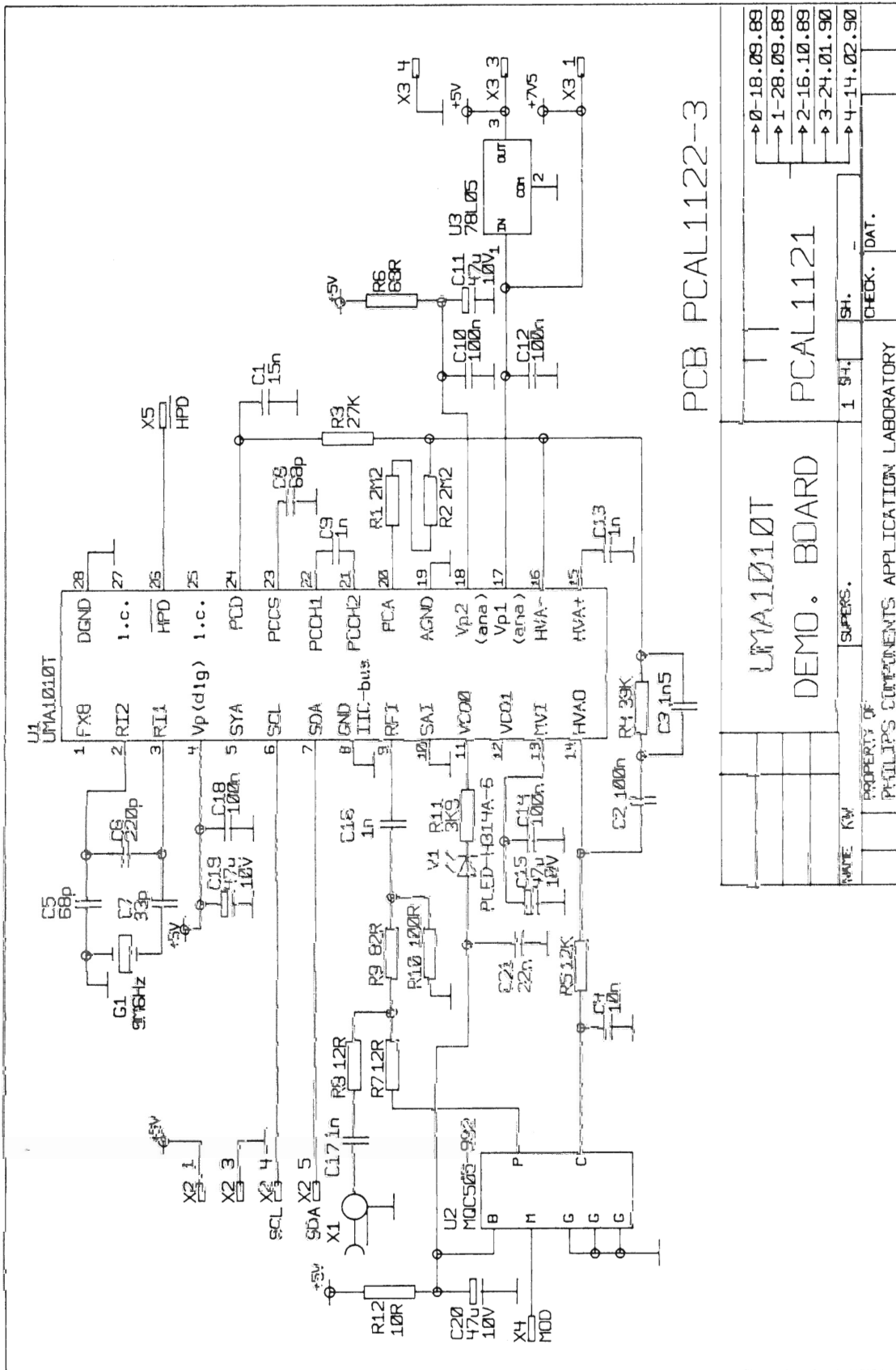


Figure 4 PCAL1122-3 demonstration board circuit diagram

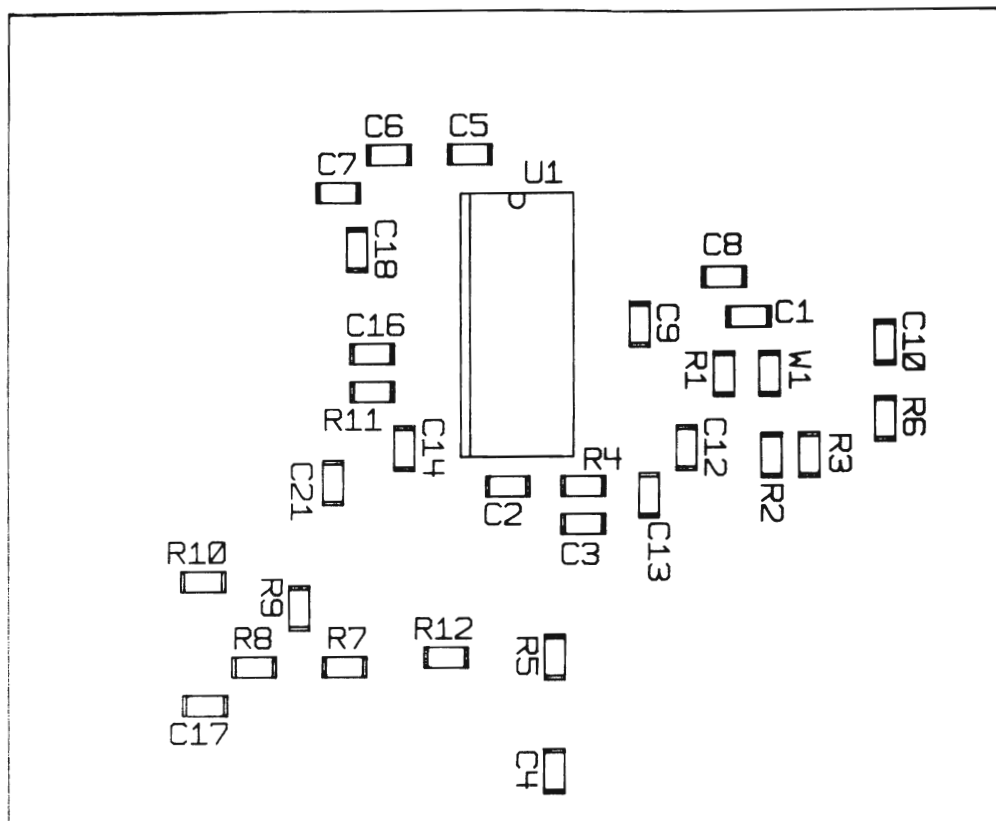


Figure 5 PCAL1122-3 demonstration board PCB layout

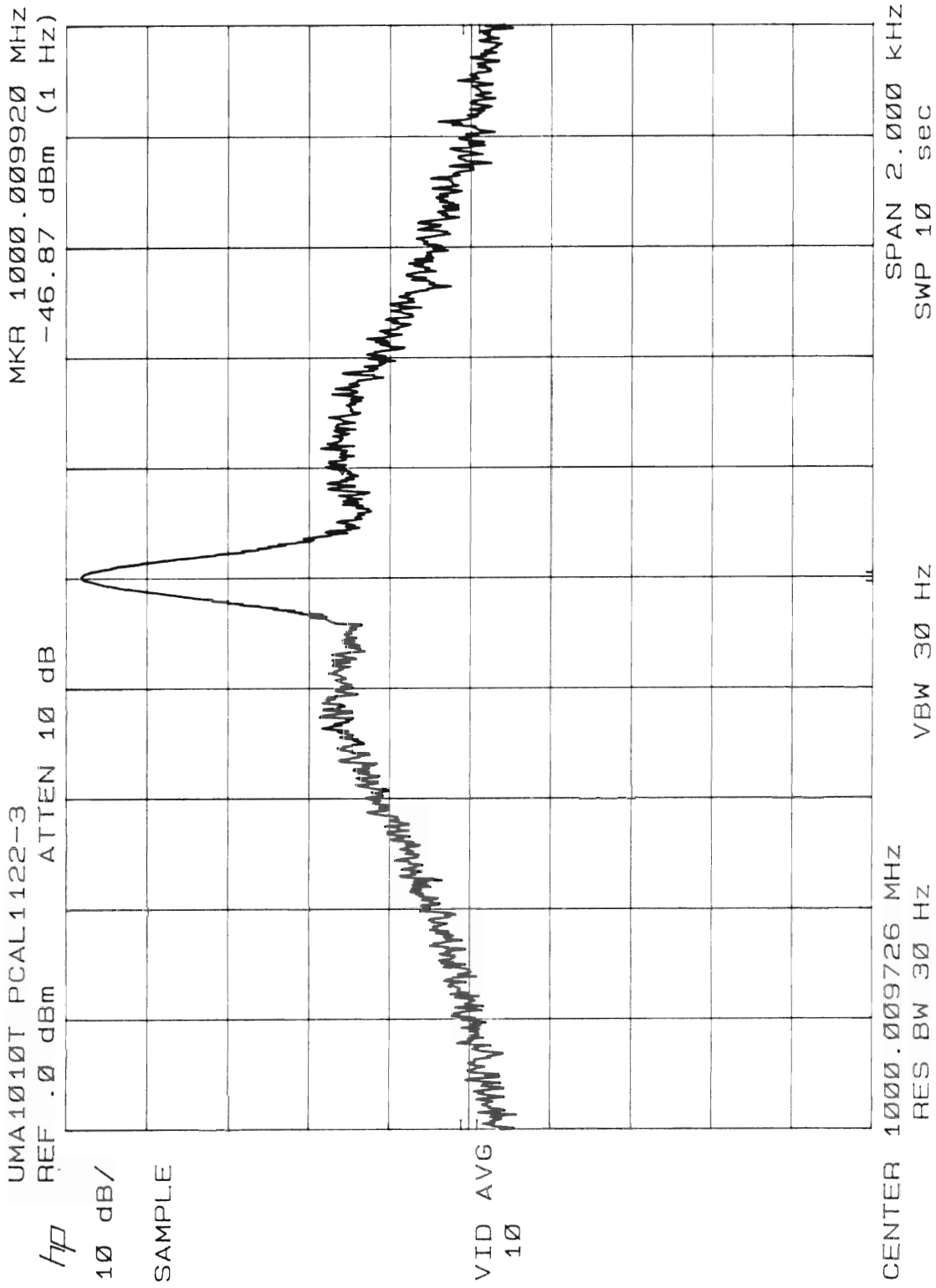


Figure 6 Typical carrier spectrum - 2kHz span

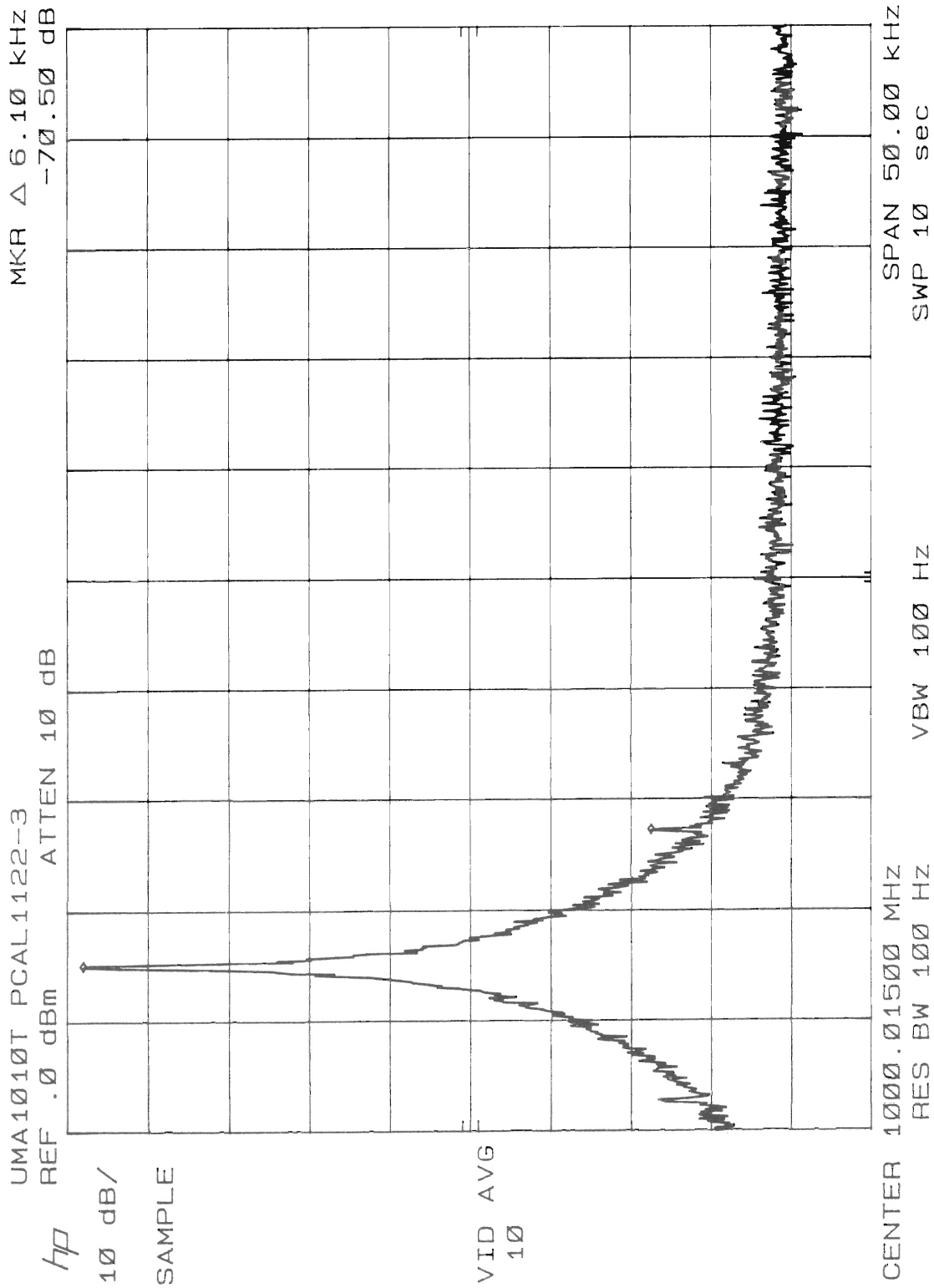


Figure 7 Typical carrier spectrum - 50kHz span

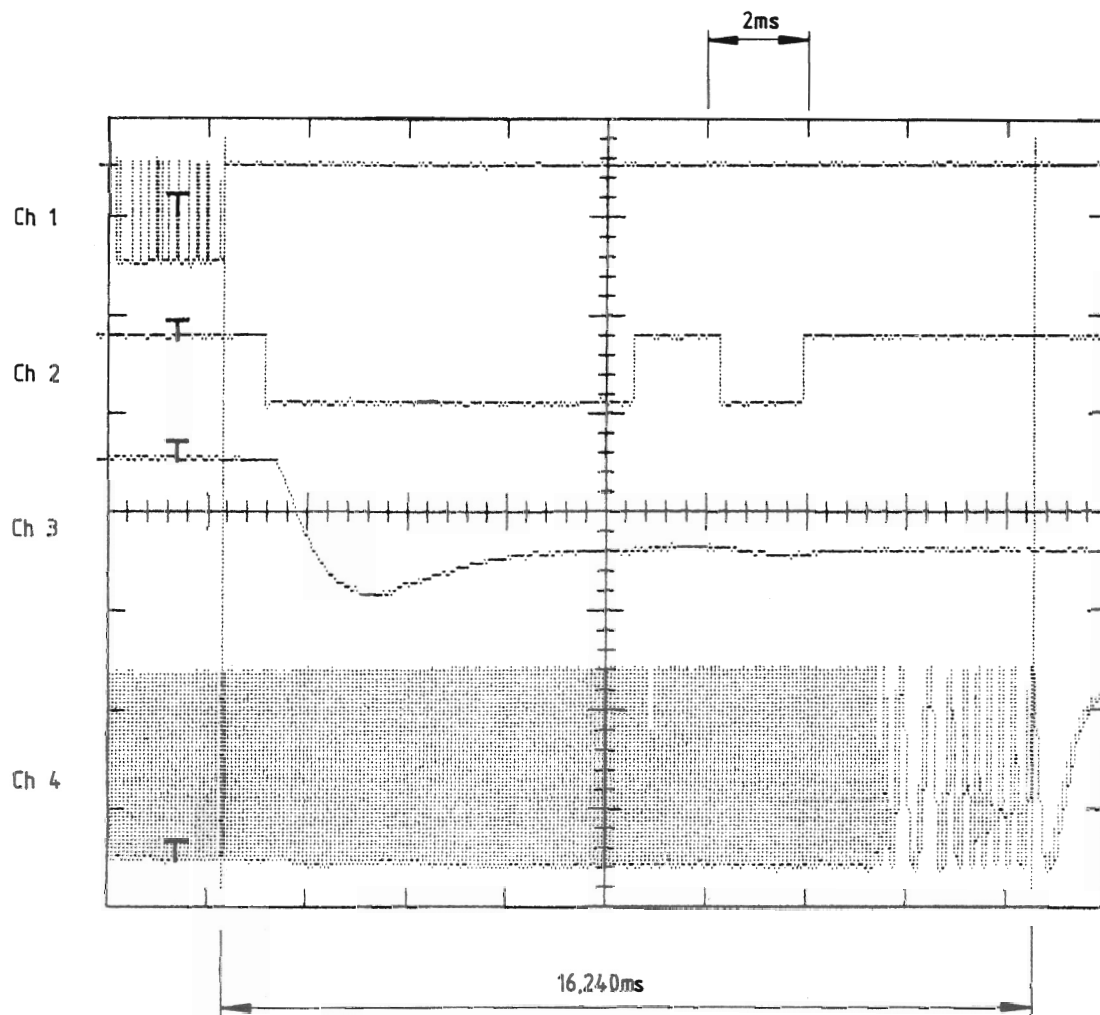


Figure 8 Typical switching waveforms

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